

FIG. 1

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MCB Address:  
0x0070030

SPR Address: 0x0030

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I n t O n l y	Any value																									SleepCNT					

FIG. 2A

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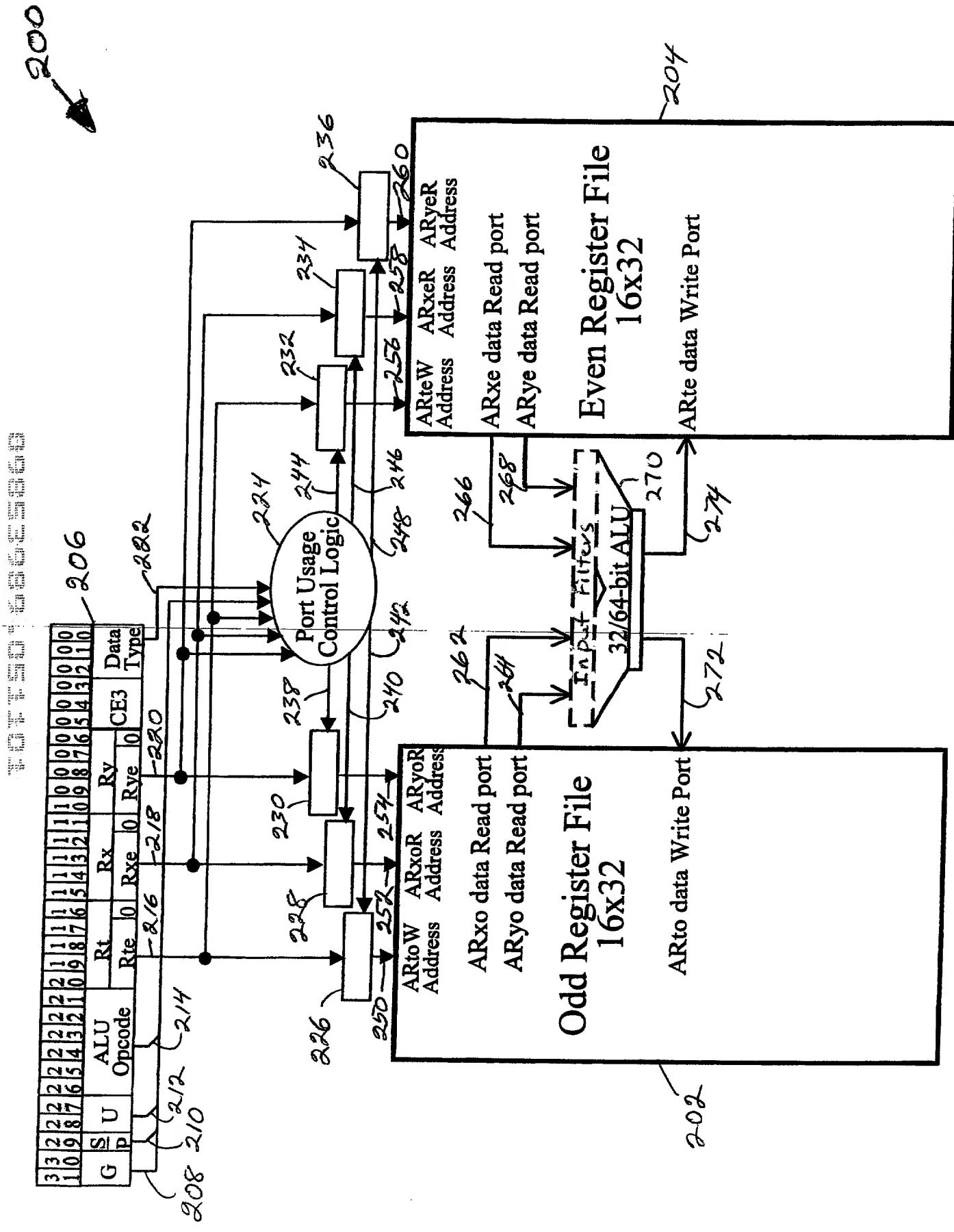
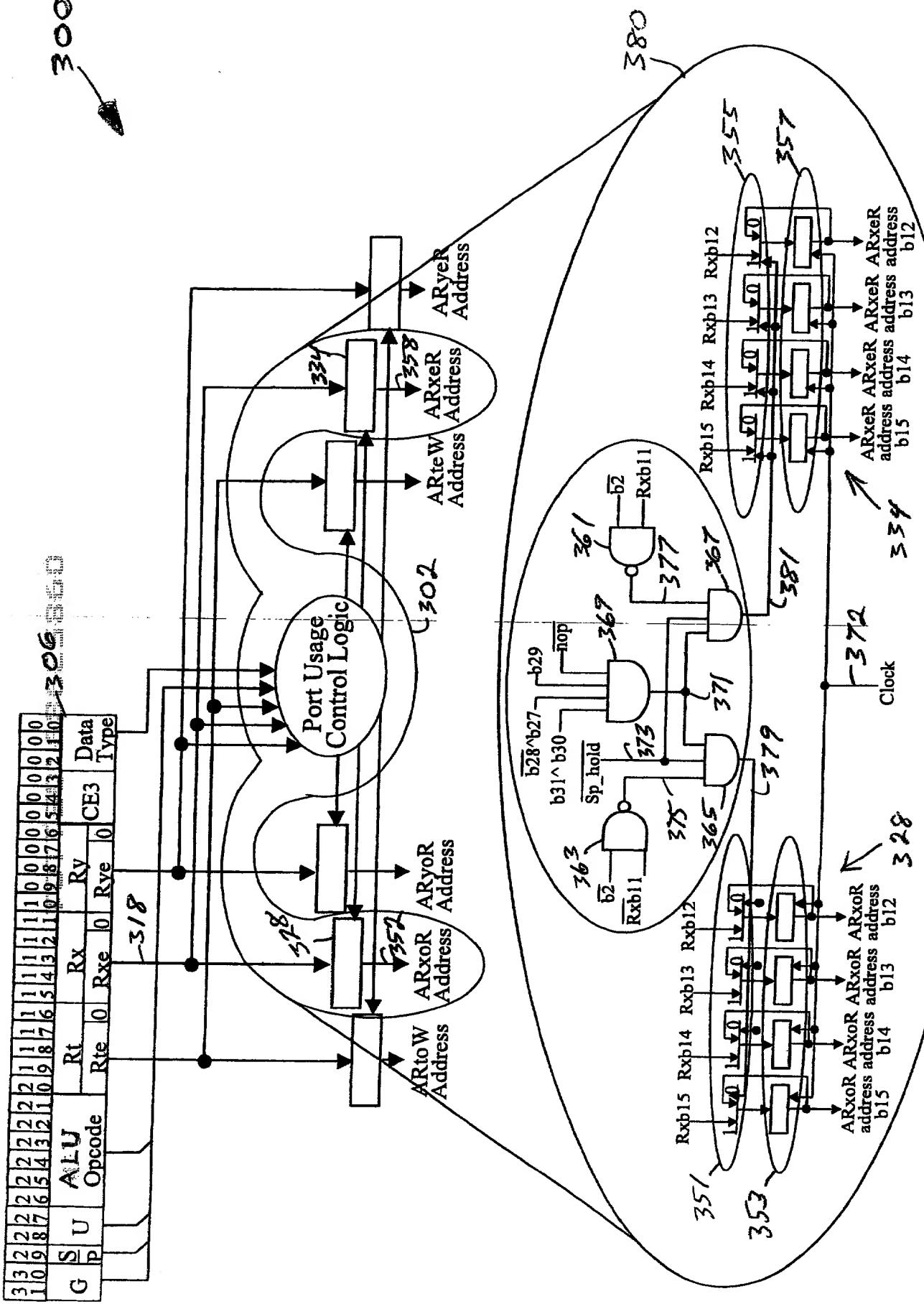


FIG. 2B

FIG. 3A



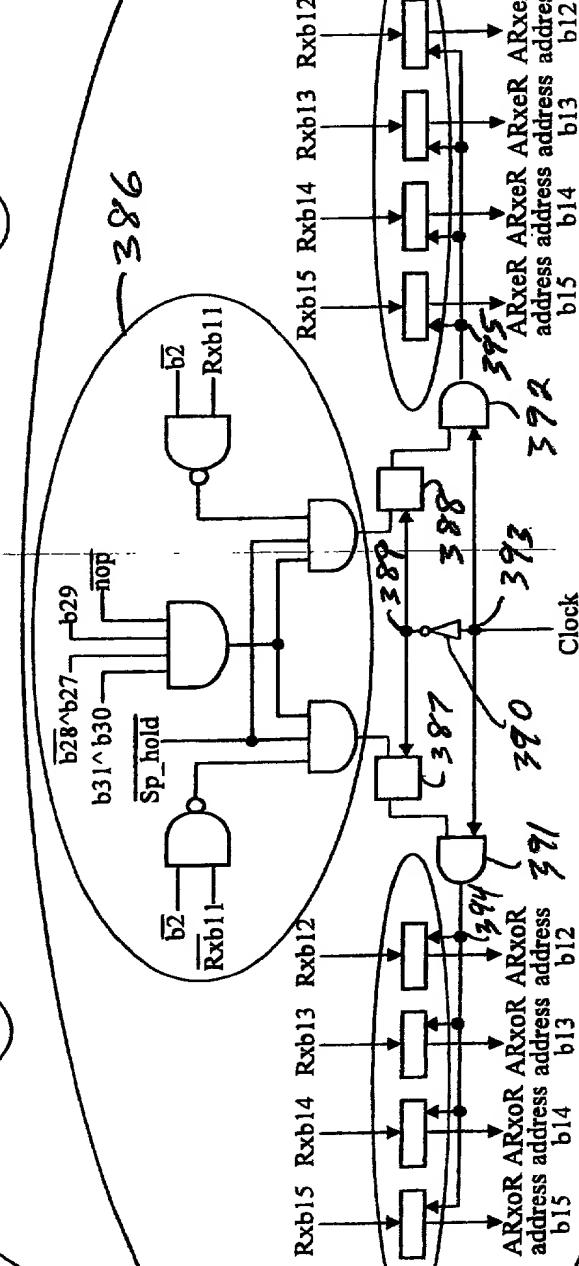
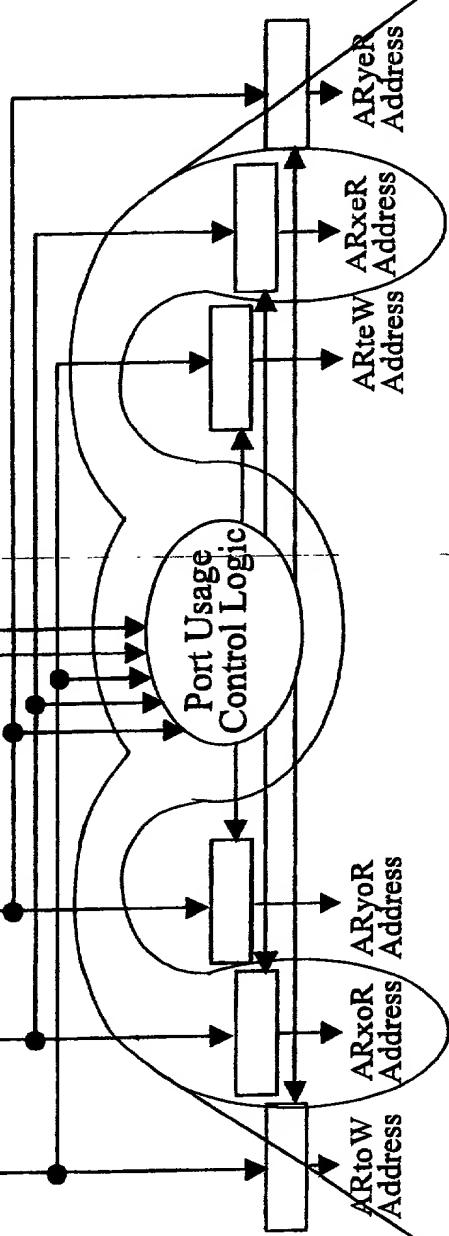
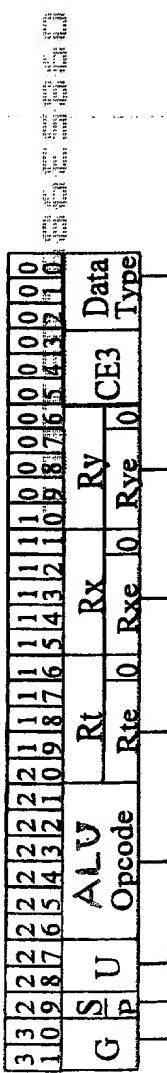


FIG. 3B

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3	3	2	2	2	2	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1			
G	S	U	P	ALU	Rt	Rx	RY	ARxo	ARyo	ARxe	ARye	ARto	MRxo	MRyo	MRto	ARxe	ARye	ARto	MRxe	MRye	MRto	ARxe	ARye	ARto	MRxe	MRye	MRto	ARxe	ARye	ARto	MRxe	MRye	MRto
3	3	2	2	2	2	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1			

400

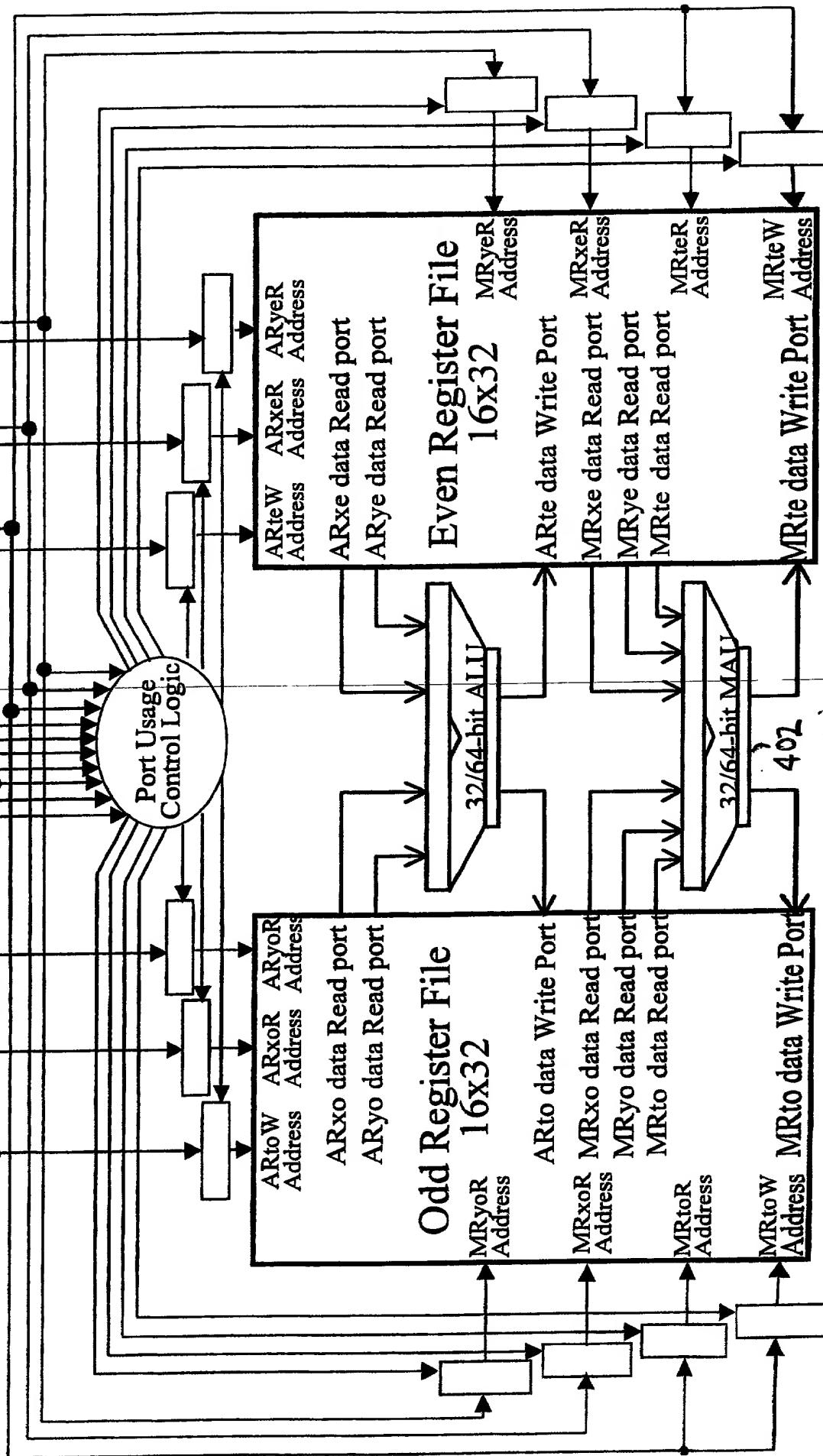


FIG. 4

### ALU Operation Encoding

		S00							
		S01							
		S02							
3	3	2	2	2	2	2	2	1	1
1	0	9	8	7	6	5	4	3	2
Group	S/ P	Unit	ALUopcode MAUopcode	Rt	Rx	Ry	Rye	CE2	DPack
				Rte	Rxe	Rye	0	0	
				0	0	0			

### Arithmetic Scalar Flags Affected (on least significant operation)

C = 1 if a carry occurs, 0 otherwise

N = MSB of result

V = 1 if an overflow occurs, 0 otherwise

Z = 1 if result is zero, 0 otherwise

See also ASF Definitions in chapter on Conditional Execution.

Cycles: 1

### Arithmetic Execution Unit ~ S04

00 = ALU

01 = MAU

10 = DSU

11 = Reserved

b<sub>23</sub> b<sub>27</sub>

FIG. 5A

D Pack

### Integer Data Packing

000 = 4 Bytes (4B)

001 = 2 Halfwords (2H)

010 = 1 Word (1W)

011 = Reserved

100 = 8 Bytes (8B)

101 = 4 Halfwords (4H)

110 = 2 Words (2W)

111 = 1 Doubleword (1D)

b<sub>23</sub>, b<sub>0</sub>

Description  
The sum of source registers Rx and Ry is stored in target register Rt.  
Syntax/Operation

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Instruction	Operands	Operation	ACF
ADD.[SP][AM].1D [TF].ADD.[SP][AM].1D	Rte, Rx, Ry Rte, Rxe, Ry	Rto  Rte $\leftarrow\right.$ Rx  Rx <sub>e</sub> + Ryo  Rye Do operation only if T/F condition is satisfied in F0	Doubleword None None
ADD.[SP][AM].1W [TF].ADD.[SP][AM].1W	Rt, Rx, Ry Rt, Rx, Ry	Rt $\leftarrow\right.$ Rx + Ry Do operation only if T/F condition is satisfied in F0	Word None None
ADD.[SP][AM].2W [TF].ADD.[SP][AM].2W	Rte, Rx, Ry Rte, Rx, Ry	Rto $\leftarrow\right.$ Rxo + Ryo Rte $\leftarrow\right.$ Rx <sub>e</sub> + Rye Do operation only if T/F condition is satisfied in F0	Dual Words None None
ADD.[SP][AM].2H [TF].ADD.[SP][AM].2H	Rt, Rx, Ry Rt, Rx, Ry	Rt.H1 $\leftarrow\right.$ Rx.H1 + Ry.H1 Rt.H0 $\leftarrow\right.$ Rx.H0 + Ry.H0 Do operation only if T/F condition is satisfied in F0	Dual Halfwords None None
ADD.[SP][AM].4H [TF].ADD.[SP][AM].4H	Rte, Rx, Ry Rte, Rx, Ry	Rto.H1 $\leftarrow\right.$ Rxo.H1 + Ryo.H1 Rto.H0 $\leftarrow\right.$ Rxo.H0 + Ryo.H0 Rte.H1 $\leftarrow\right.$ Rx <sub>e</sub> .H1 + Rye.H1 Rte.H0 $\leftarrow\right.$ Rx <sub>e</sub> .H0 + Rye.H0 Do operation only if T/F condition is satisfied in F0	Quad Halfwords None None
ADD.[SP][AM].4B [TF].ADD.[SP][AM].4B	Rt, Rx, Ry Rt, Rx, Ry	Rt.B3 $\leftarrow\right.$ Rx.B3 + Ry.B3 Rt.B2 $\leftarrow\right.$ Rx.B2 + Ry.B2 Rt.B1 $\leftarrow\right.$ Rx.B1 + Ry.B1 Rt.B0 $\leftarrow\right.$ Rx.B0 + Ry.B0 Do operation only if T/F condition is satisfied in F0	Quad Bytes None None
ADD.[SP][AM].8B [TF].ADD.[SP][AM].8B	Rte, Rx, Ry Rte, Rx, Ry	Rto.B3 $\leftarrow\right.$ Rxo.B3 + Ryo.B3 Rto.B2 $\leftarrow\right.$ Rxo.B2 + Ryo.B2 Rto.B1 $\leftarrow\right.$ Rxo.B1 + Ryo.B1 Rto.B0 $\leftarrow\right.$ Rxo.B0 + Ryo.B0 Rte.B3 $\leftarrow\right.$ Rx <sub>e</sub> .B3 + Rye.B3 Rte.B2 $\leftarrow\right.$ Rx <sub>e</sub> .B2 + Rye.B2 Rte.B1 $\leftarrow\right.$ Rx <sub>e</sub> .B1 + Rye.B1 Rte.B0 $\leftarrow\right.$ Rx <sub>e</sub> .B0 + Rye.B0 Do operation only if T/F condition is satisfied in F0	Dual Bytes None None

Fig. 5B

## MPYA - Multiply Accumulate

Encoding	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Group	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
S/P																																		
Unit																																		
MAUopcode	Rte	0	Rx	Ry	CE3	MPack																												

FIG. 6A

Syntax/Operation	Instruction	Operands	Operation	ACF
MPYA.[SPIM.1 SU]W	Rte, Rx, Ry	Do operation below but do not affect ACFs	Word	None
MPYA.[CNVZ].[SPIM.1 SU]W	Rte, Rx, Ry	Rto Rte $\leftarrow$ Rto  Rte + (Rx * Ry)	F0	
[TF].MPYA.[SPIM.1 SU]W	Rte, Rx, Ry	Do operation only if T/F condition is satisfied in ACFs	None	
			Dual Halfwords	
MPYA.[SPIM.2 SU]H	Rte, Rx, Ry	Do operation below but do not affect ACFs	None	
MPYA.[CNVZ].[SPIM.2 SU]H	Rte, Rx, Ry	Rto $\leftarrow$ Rto + (Rx.H1 * Ry.H1)	F1	
[TF].MPYA.[SPIM.2 SU]H	Rte, Rx, Ry	Rte $\leftarrow$ Rte + (Rx.H0 * Ry.H0)	F0	
			Do operation only if T/F condition is satisfied in ACFs	None
MPYA.[SPIM.4 SU]B	Rte, Rx, Ry	Do operation below but do not affect ACFs	Quad Bytes	None
MPYA.[CNVZ].[SPIM.4 SU]B	Rte, Rx, Ry	Rto.H1 $\leftarrow$ Rto.H1 + (Rx.B3 * Ry.B3)	F3	
		Rto.H0 $\leftarrow$ Rto.H0 + (Rx.B2 * Ry.B2)	F2	
		Rte.H1 $\leftarrow$ Rte.H1 + (Rx.B1 * Ry.B1)	F1	
		Rte.H0 $\leftarrow$ Rte.H0 + (Rx.B0 * Ry.B0)	F0	
[TF].MPYA.[SPIM.4 SU]B	Rte, Rx, Ry	Do operation only if T/F condition is satisfied in F0		None

FIG. 6C

## Arithmetic Scalar Flags Affected (on least significant operation)

C = Not affected

N = MSB of result

V = Not affected

Z = 1 if result is zero, 0 otherwise

Cycles: 2

## Arithmetic Execution Unit

00 = ALU

01 = MAU

10 = DSU

11 = Reserved

b<sub>25</sub>b<sub>24</sub>

b<sub>23</sub>b<sub>22</sub>

FIG. 6C

## Mpack - Multiply Data Packing

000 = Reserved

001 = 2 Halfwords (2H)

010 = 1 Word (1W)

011 = Reserved

100 = Reserved

101 = 4 Halfwords (4H) for MPYH and MPYL

110 = Reserved

111 = Reserved

b<sub>1</sub>b<sub>0</sub>b<sub>2</sub>  
SP/PE Select

0 = SP

1 = PE

b<sub>3</sub>b<sub>2</sub>b<sub>1</sub>

FIG. 6D

## Instruction Group

00 = Reserved

01 = Flow Control

10 = Load/Store (LU, SU)

11 = Arithmetic/Logical (ALU, MAU, DSU)

b<sub>2</sub>b<sub>1</sub>b<sub>0</sub>

b<sub>3</sub>b<sub>2</sub>b<sub>1</sub>

b<sub>4</sub>b<sub>3</sub>b<sub>2</sub>

b<sub>5</sub>b<sub>4</sub>b<sub>3</sub>

b<sub>6</sub>b<sub>5</sub>b<sub>4</sub>

b<sub>7</sub>b<sub>6</sub>b<sub>5</sub>

b<sub>8</sub>b<sub>7</sub>b<sub>6</sub>

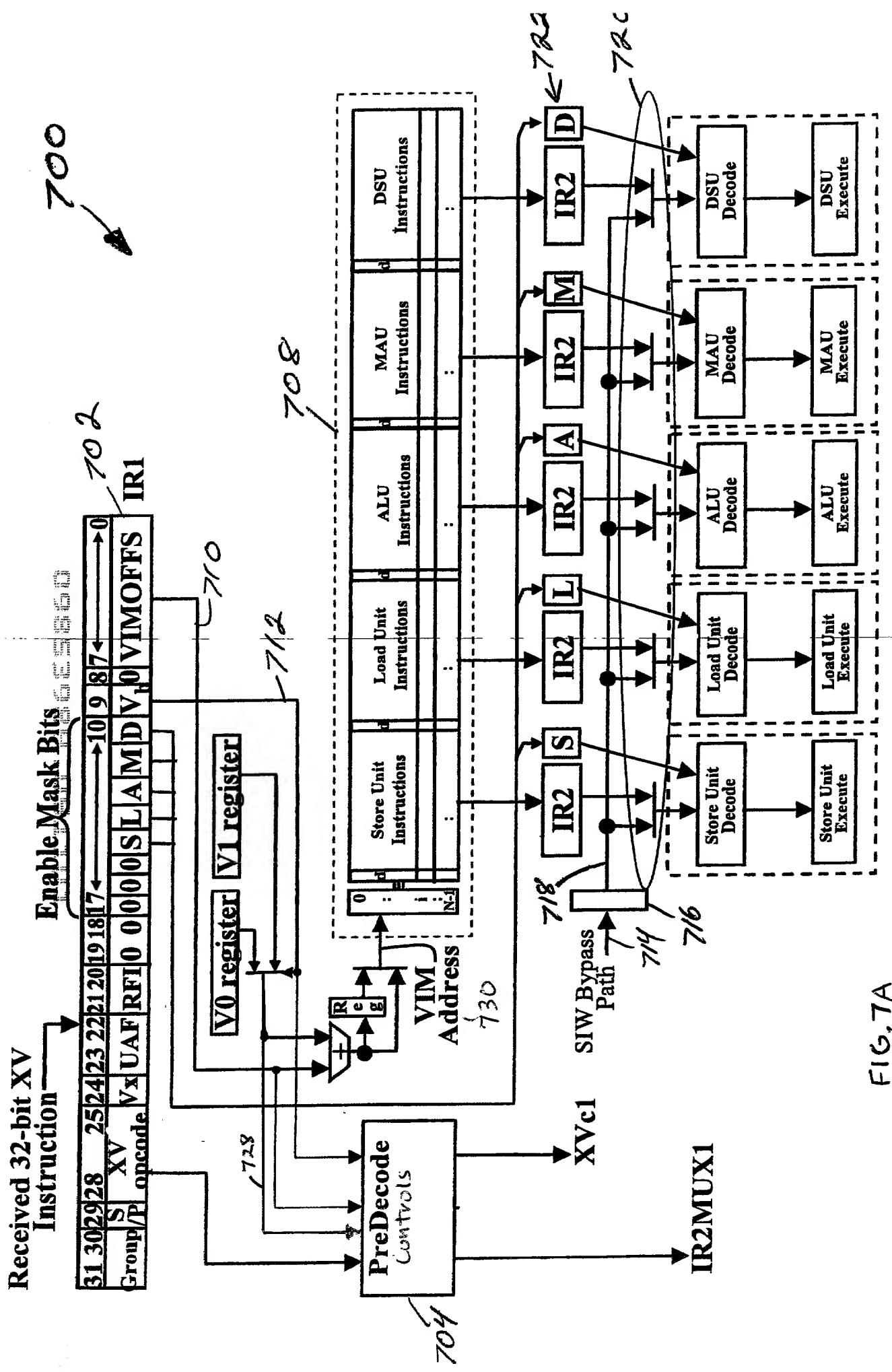
b<sub>9</sub>b<sub>8</sub>b<sub>7</sub>

b<sub>10</sub>b<sub>9</sub>b<sub>8</sub>

b<sub>11</sub>b<sub>10</sub>b<sub>9</sub>

b<sub>12</sub>b<sub>11</sub>b<sub>10</sub>

FIG. 6C



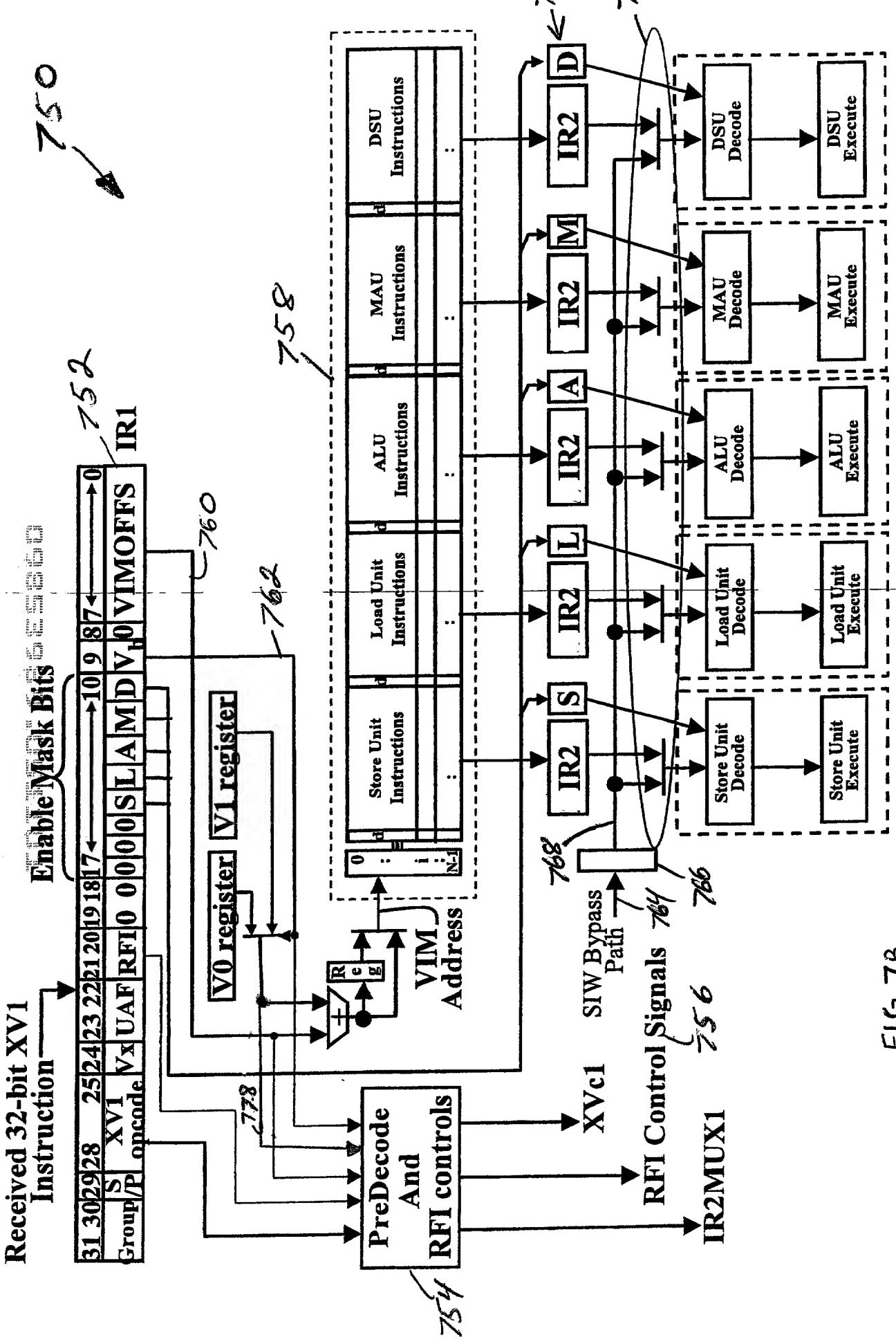


FIG. 7B

Received 32-bit XV2  
Instruction

31	30	29	28	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
S	XV2	Group/P	opcode	UAF	RFI	V1 <sub>n</sub>	SOFs	LOFS	AOFs	AOFS	MOFS	DOFS																		

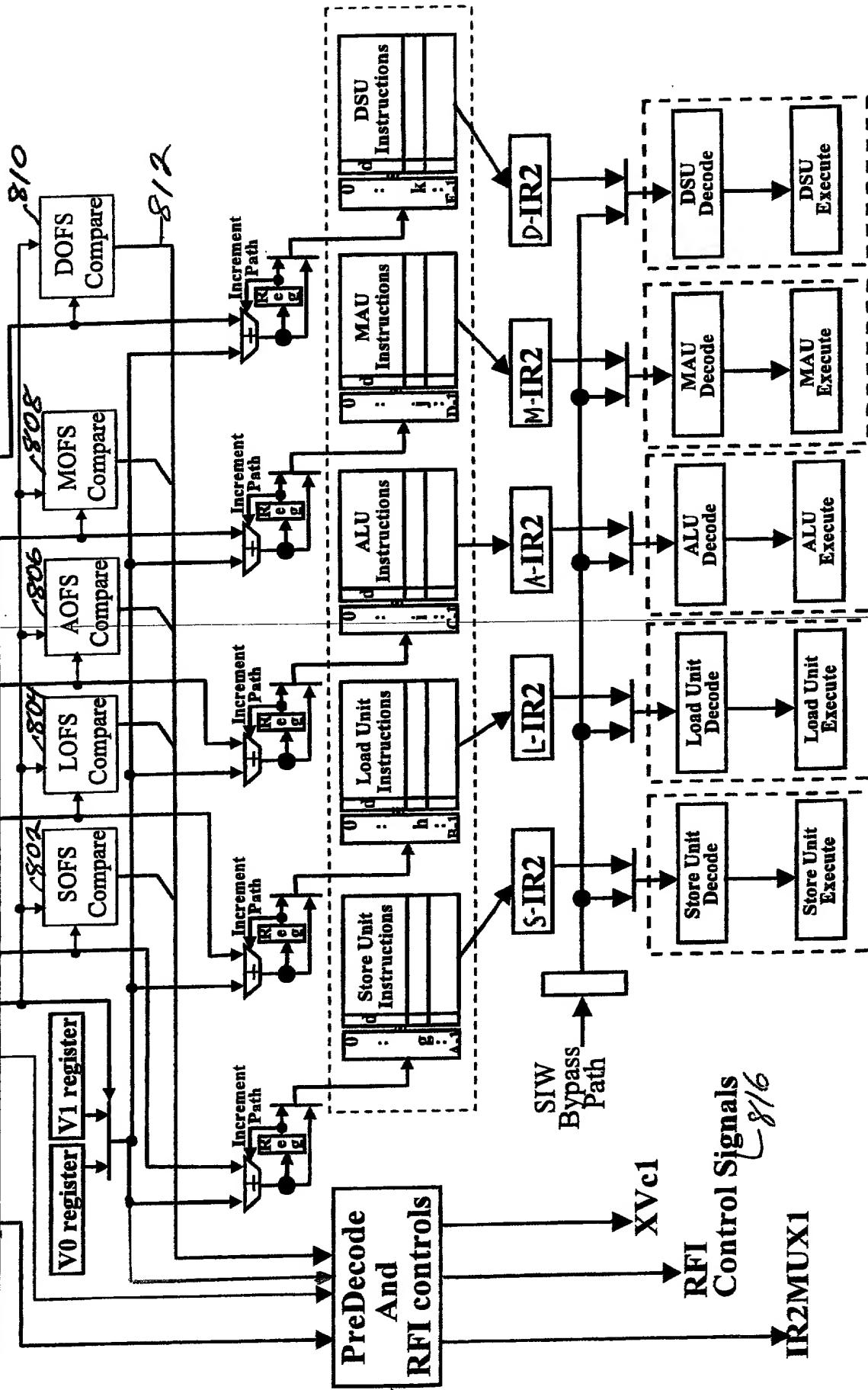


FIG. 8